## PROTECT YOUR WAFERS

The most valuable product in the semiconductor and electronics industry is also the most fragile and susceptible to mishandling and contamination. Mix in that not all wafers are created equal, which means one product does not fit all wafers! POLOS® offers various solutions to safely ship and store your wafers; from single wafer shipping shippers, wafer boxes, wafer containers, wafer carrier trays to coin style and clamshell shippers.



From the most advanced eLX wafer canisters to cost-efficient wafer jars, we offer tailor fit products to meet your requirements. Our coin style and clamshell shippers keep the wafers secure and only contact the edges of the wafer during shipping and storage.

The single wafer shippers are available in different sizes 1", 1.5", 2", 2.5", 3", 4", 5" and 6" and in materials Natural PP or ESD-Safe Conductive PP. They are impact resistant with a screw-on lid for secure packing. Available from stock! Contact us for special requests!

Wafer size	ePAK description	Internal diameter	Order code
1" (25 mm)	eCT1-25-ASSY-1-eM-08-NAT	25.4 mm	eWB0091-ASSY-1
1.5" (38 mm)	eCT1.5-38-ASSY-1-eM-08-NAT	39.6 mm	eWB0325-ASSY-1
2" (50 mm)	eCT2-50-ASSY-1-eM-08-NAT	52 mm	eWB0021-ASSY-1
2.5" (63 mm)	eCT2.5-63-ASSY-1-eM-08-NAT	65.5 mm	eWB0328-ASSY-1
3" (76 mm)	eCT3-76-ASSY-1-eM-08-NAT	78.6 mm	eWB0022-ASSY-1
4" (100 mm)	eCT4-100-ASSY-1-eM-08-NAT	104 mm	eWB0024-ASSY-1
5" (125 mm)	eCT5-125-ASSY-1-eM-08-NAT	127 mm	eWB0060-ASSY-1
6" (150 mm)	eCT6-150-ASSY-1-eM-08-NAT	152 mm	eWB0025-ASSY-1





Process boats and storage boxes for 2, 3, 4, 6 and 8" wafers. Designed with open or closed slots to ensure easy and safe wafer handling.



Wafer shipping boxes for 1, 2, 2,5, 3, 4, 6 and 8" wafers. Designed to hold multiple wafers by the edge.



Plastic wafer jars, with foams and wafer separators and liners for easy loading / unloading in automated or manual applications.



ELX wafer canisters enhanced protection of wafer surfaces. Minimizes lateral movement without applying compression to delicate wafer edges.